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**Republic of Iraq**

**Ministry of Higher Education**

**& Scientific Research**

**University: Diyala University**

**College: College of Engineering**

**Department: Electronic Engineering**

**Stage: fourth**

**Lecturer name:** Qahtan Khalaf Omran

**Qualification: PhD**

**Place of work: Electronic Dept.**

**(( Annual teaching plan form))**

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| **Lecturer Name** | Qahtan Khalaf Omran |
| **Email** | **Khatan khalafo@yahoo.com** |
| **Subject** | Digital System Design |
| **Aims** | **The aim of this subject is to make the students ready to undestand and comprehend the scientific theories and their applications related to their field of the study.** |
| **Textbooks** | DIGITAL DESIGN BY MORISANO M |
| **Additional Textbooks** | DIGITAL DESIGN BY FLOD |
| **Assessments** | **First Semester** | **Second Semester** | **Laboratory** | **Final Exam** |
| 20% | 20% |  | 60% |
| **Notes** |  |

**Schedule Weekly Lessons - First Semester**

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| --- | --- | --- | --- | --- |
| **Week** | **Date** | **Lectures** | **Lab. Experments** | **Notes** |
| 1 | **29/9/** | Simplification of Boolean Function using K-map and Tabulation |  |  |
| 2 | **5/10/** | Simplification of Boolean Function using K-map and Tabulation |  |  |
| 3 | **12/10/** | Simplification of Boolean Function using K-map and Tabulation |  |  |
| 4 | **19/10/** | Digital Circuit Design using Logic Circuits (LSI, SSI, MSI) |  |  |
| 5 | **26/10/** | Digital Circuit Design using Logic Circuits (LSI, SSI, MSI) |  |  |
| 6 | **2/11/** | Digital Circuit Design using Logic Circuits (LSI, SSI, MSI) |  |  |
| 7 | **9/11/** | Design using Programmable Logic Circuits (ROM, PLA, PAL) |  |  |
| 8 | **16/11/** | Design using Programmable Logic Circuits (ROM, PLA, PAL) |  |  |
| 9 | **23/11/** | Design using Programmable Logic Circuits (ROM, PLA, PAL) |  |  |
| 10 | **30/11/** | Synchronized Sequential Circuits (Analysis and Design) |  |  |
| 11 | **7/12/** | Synchronized Sequential Circuits (Analysis and Design) |  |  |
| 12 | **14/12/** | Synchronized Sequential Circuits (Analysis and Design) |  |  |
| 13 | **21/12/** | ASM Diagrams |  |  |
| 14 | **28/12/** | ASM Diagrams |  |  |
| 15 | **4/1/** | ASM Diagrams |  |  |
| 16 | **11/1/** | **ASM Diagrams** |  |  |
| Half Year holiday | 15/1/ to1/2/ |  |  |  |

**Lecturer Signature Head of Dept. Signature Dean Signature**

**Schedule Weekly Lessons - Second Semester**

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| **Week** | **Date** | **Lectures** | **Lab. Experments** | **Notes** |
| 1 | **15/2/** | Analysis and Design of Sequential Circuits using ASM Diagrams |  |  |
| 2 | **22/2/** | Analysis and Design of Sequential Circuits using ASM Diagrams |  |  |
| 3 | **1/3/** | Analysis and Design of Sequential Circuits using ASM Diagrams |  |  |
| 4 | **8/3/** | Asynchronous Circuits (Analysis) |  |  |
| 5 | **15/3/** | Asynchronous Circuits (Analysis) |  |  |
| 6 | **22/3/** | Asynchronous Circuits (Analysis) |  |  |
| 7 | **29/3/** | Luminescent pulse phenomenon in logic circuits (Static and Dynamic |  |  |
| 8 | **5/4/** | Luminescent pulse phenomenon in logic circuits (Static and Dynamic |  |  |
| 9 | **12/4/** | Luminescent pulse phenomenon in logic circuits (Static and Dynamic |  |  |
| 10 | **19/4/** | Microprocessors-Component and Architecture |  |  |
| 11 | **26/4/** | Microprocessors-Component and Architecture |  |  |
| 12 | **3/5/** | Microprocessors-Component and Architecture |  |  |
| 13 | **10/5/** | Microprocessors Hardwer, 4-, 8-, 16- and 32-bit Microprocessors |  |  |
| 14 | **17/5/** | Microprocessors Hardwer, 4-, 8-, 16- and 32-bit Microprocessors |  |  |
| 15 | **24/5/** | Single Chip Microcomputer 8085, 8088, MPU details. |  |  |
| 16 | **1/6/** | Single Chip Microcomputer 8085, 8088, MPU details. |  |  |

**Lecturer Signature Head of Dept. Signature Dean Signature**